1. An interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors, the interface comprising:

an instruction bus, configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU; and

a data bus, coupled to said instruction bus, configured to subsequently transfer the data, wherein data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order.

2. The interface as recited in claim 1 wherein the plurality of coprocessors comprises:

a first plurality of floating-point coprocessors; or

a first plurality of 3-D graphics accelerators; or

a second plurality of floating-point coprocessors and a second plurality of 3-D graphics accelerators.

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1 3.   The interface as recited in claim 1, wherein said

2   particular instructions comprise TO instructions, said

3   TO instructions directing that the subsequent transfer

4   of the data will be from the CPU to said designated

5   ones of the plurality of coprocessors.

1 4.   The interface as recited in claim 3, wherein said

2   particular instructions comprise FROM instructions,

3   said FROM instructions directing that the subsequent

4   transfer of the data will be to the CPU from said

5   designated ones of the plurality of coprocessors.

1 5.   The interface as recited in claim 4, wherein said data

2   bus comprises:

3   data TO signals, for transferring data from the CPU to

4   said designated ones of the plurality of

5   coprocessors; and

6   data FROM signals, for transferring data to the CPU

7   from said designated ones of the plurality of

8   coprocessors.

1 6.   The interface as recited in claim 5, wherein said data

2   order signals comprise:

3   TO order signals, for prescribing said data transfer

4   order with respect to transfers via said data TO

5   signals; and

6   FROM order signals, for prescribing said data transfer

7   order with respect to transfers via said data

8   FROM signals.

1 7. The interface as recited in claim 6, wherein said TO

2   order signals prescribe a particular outstanding TO

3   instruction relative to all outstanding TO

4   instructions.

1 8. The interface as recited in claim 6, wherein said FROM

2   order signals prescribe a particular outstanding FROM

3   instruction relative to all outstanding FROM

4   instructions.

1 9. The interface as recited in claim 1 wherein said data

2   bus transfers the data in parallel to one of said

3   designated ones of the plurality of coprocessors, said

4   one of said designated ones of the plurality of

5   coprocessors having multiple issue pipelines providing

6   for parallel instruction execution.

1 10. A computer program product for use with a computing

2   device, the computer program product comprising:

3   a computer usable medium, having computer readable

4   program code embodied in said medium, for causing

5   a coprocessor interface to be described that

6   transfers data between CPU and a plurality of

7   coprocessors, said computer readable program code

8   comprising:

9   first program code, for providing an instruction

10   bus, said instruction bus configured to

11   transfer instructions to said plurality of

12   coprocessors in an instruction transfer

13   order, wherein particular instructions

14   direct designated ones of the plurality of

15   coprocessors to transfer said data to/from

16   said CPU; and

17   second program code, for providing a data bus,

18   said data bus configured to subsequently

19   transfer said data, wherein data order

20   signals within said data bus prescribe a

21   data transfer order that is different from

22   said instruction transfer order.

1 11. The computer program product as recited in claim 10,

2   wherein said particular instructions comprise:

3   TO instructions, said TO instructions directing that

4   the subsequent transfer of said data will be from

5   said CPU to said designated ones of said

6   plurality of coprocessors; and

7   FROM instructions, said FROM instructions directing

8   that the subsequent transfer of said data will be

9   to said CPU from said designated ones of said

10   plurality of coprocessors.

1   12. The computer program product as recited in claim 11,

2   wherein said data order signals comprise:

3   TO order signals, for specifying said data transfer

4   order for a particular outstanding TO instruction

5   relative to all outstanding TO instructions; and

6   FROM order signals, for specifying said data transfer

7   order for a particular outstanding FROM

8   instruction relative to all outstanding FROM

9   instructions.

1   13. The computer program product as recited in claim 10,

2   data bus is configured to transfer said data in

3   parallel to particular coprocessors that have multiple

4   issue pipelines providing for parallel instruction

5   execution and corresponding data transfers.

1   14. A computer data signal embodied in a transmission

2   medium, the computer data signal comprising:

3   computer-readable first program code, for providing an

4   instruction bus for transferring instructions to

5   a plurality of coprocessors in an instruction

6   transfer order, wherein particular instructions

7   direct particular coprocessors to transfer data

8   to/from a CPU; and

9   computer-readable second program code, for providing a

10   data bus for subsequently transferring said data,

11   wherein data order signals within said data bus

12   prescribe a data transfer order that differs from

13   said instruction transfer order.

1   15. The computer data signal as recited in claim 14,

2   wherein said particular instructions comprise TO

3   instructions, said TO instructions directing that

4   subsequent transfer of said data will be from said CPU

5   to said particular coprocessors.

1   16. The computer data signal as recited in claim 15,

2   wherein said particular instructions comprise FROM

3   instructions, said FROM instructions directing that

4   the subsequent transfer of said data will be to said

5   CPU from said particular coprocessors.

1 17. The computer data signal as recited in claim 14,

2   wherein said data bus comprises:

3   data TO signals, for transferring data from said CPU

4   to said particular coprocessors; and

5   data FROM signals, for transferring data to said CPU

6   from said particular coprocessors.

1 18. The computer data signal as recited in claim 17,

2   wherein said data order signals comprise:

3   TO order signals, for prescribing said data transfer

4   order with respect to transfers via said data TO

5   signals; and

6   FROM order signals, for prescribing said data transfer

7   order with respect to transfers via said data

8   FROM signals.

1 19. The computer data signal as recited in claim 18,

2   wherein said TO order signals prescribe a particular

3   outstanding TO instruction relative to all outstanding

4   TO instructions.

1 20. The computer data signal as recited in claim 18,

2   wherein said FROM order signals prescribe a particular

3   outstanding FROM instruction relative to all

4   outstanding FROM instructions.

1 21. The computer data signal as recited in claim 1 wherein

2   said data bus transfers said data in parallel to

3   selected coprocessors, said selected coprocessors

4   having multiple issue execution pipelines.

1 22. A method for transferring data between a CPU and a

2   plurality of coprocessors, the method comprising:

3   a) transmitting instructions to the plurality

4   coprocessors, each of the instructions directing

5   a data transfer between the CPU and a specific

6   coprocessor, wherein said transmitting is

7   provided in a specific instruction order;

8   b) subsequently transferring the data in an order

9   different from the specific instruction order,

10   said transferring comprising:

11   i) prescribing transfer of a data element

12   corresponding to a specific outstanding

13   instruction relative to all outstanding

14   instructions, the outstanding instructions

15   being those instructions that have not

16   completed a subsequent data transfer.

1 22. The method as recited in claim 21, said transmitting

2   comprises:

3   i) issuing a plurality of the instructions in parallel

4   to the specific coprocessor; and

5   ii) designating an execution order corresponding to

6   said issuing.